REMARKS

Claims 1-14 and 16-30 are pending for examination with claims 1, 8, 16, 22, 27 and 28 being independent claims. No claims have been amended and no new matter has been added.

Rejections Under 35 U.S.C. §102

Claims 1-14 and 16-30 stand rejected under 35 U.S.C. §102(e) as being anticipated by Özlütürk (U.S. Patent No. 6,366,607). Applicant respectfully disagrees and traverses as follows.

Özlütürk is directed to a process for improved performance of a data signal decoder. (Abstract). Özlütürk teaches employing a phase-locked loop to eliminate errors due to carrier-offset. (Abstract). Özlütürk teaches signal despreading using a rake receiver and multiple Viterbi decoders (see Fig. 4).

Claim 1 is representative of the independent claims. Claim 1 recites:

1. A method for processing signal values in a digital signal processor, the method comprising:

in response to a single instruction that specifies a plurality of signal values and a plurality of code segments of a despreading code:

complex multiplication of each signal value by a respective one of the code segments to provide a plurality of intermediate results;

complex addition of the intermediate results to provide a despread result; and

storing the despread result, wherein the complex multiplication, the complex addition and the storing of the despread result are executed in a single clock cycle of the digital signal processor.

The method of claim 1 requires that a number of actions be executed in response to a single instruction. In addition claim 1 requires that the complex addition and storing of the despread result be executed in a single clock cycle of the digital signal processor. Özlütürk does not disclose or suggest executing the actions of claim 1 in response to a single instruction, nor does Özlütürk disclose or suggest executing the complex multiplication, complex addition and the storing of the despread result within a single clock cycle of the digital signal processor.

Indeed, the structure of Özlütürk is such that performing those actions within a single clock cycle is not possible. Referring to Özlütürk Fig. 5, for each rake element the pn code sequence is delayed by one chip and mixed with the baseband spread spectrum signal to achieve despreading. (Col. 4, lines 61-64). Özlütürk then states that:

> Each multiplication product is input in an accumulator 109_0, 109_1, 109_2, 109_n, where it is added to the previous product and latched out after the next symbol-clock cycle.

(Col. 4, lines 64-67). As shown in Fig. 5, these accumulators are structured to continue taking input from the complex mixer 107 and to add the results of the mixing in successive clock cycles. The accumulators of Özlütürk are not structured to execute these actions within a single clock cycle. Single clock cycle operation is not contemplated by Özlütürk, or possible given the accumulator structure taught. Özlütürk specifically teaches that inputting a product into an accumulator and adding it to a previous product takes at least two clock cycles. Özlütürk requires a plurality of clock cycles to process the plurality of signal values recited by claim 1. Claim 1 requires that the process be executed in a single clock cycle. Özlütürk therefore specifically teaches away from this limitation of claim 1.

Furthermore, nowhere does Özlütürk disclose or suggest performing a number of operations in response to a single instruction, let alone disclose or suggest performing the specific operations required by claim 1 in response to a single instruction.

Claim 1 requires the complex multiplication, complex addition and storing all be performed in response to a single instruction. Claim 1 further requires that the complex multiplication, the complex addition and the storing of the despread result are executed in a single clock cycle of the digital signal processor. Özlütürk does not disclose or suggest either of these limitations. Claim 1 is therefore patentable over Özlütürk for at least this reason.

The remaining independent claims, 8, 16, 22, 27 and 28, also contain similar limitations regarding the execution of operations in response to a single instruction and within a single clock cycle. Those claims are therefore patentable for at least the same reason described above in reference to claim 1. The dependent claims are therefore patentable for at least the same reason.

Accordingly, withdrawal of the rejection is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
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